REMARKS/ARGUMENTS

Claims 4 and 7-14 are canceled. Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Stein (US Patent 4,725,747) in view of Matsuo et al. (US Patent 5,744,838). Claim 1 is amended to include the limitations of claim 4 and further to recite, in part, "...the gate structure being configured to receive an external signal...". Support for this limitation is provided, for example, in Fig. 9, where external signal 906 is shown as being applied to gate 904. Reconsideration of the rejections of claims 1-3 and 5-6 is respectfully requested.

In Stein, gate structures 24 and 16 receive internal signals and not external signals. In contrast, claim 1 is amended to recite, in part, "a gate structure overlaying the conduction channels, the gate structure being configured to receive an external signal...." Therefore, neither Stein, nor Matsuo, whether taken alone or in combination, teach or suggest claim 1, as amended.

Furthermore, in making these rejections, the Examiner asserts:

.....It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a plurality of diodes in order to "prevent a gate oxide film of the initial input stage logic circuit from deterioration or breaking by reducing the value of the surge voltage" [column 1-2, lines 68-3] or to increase gate capacitance....

Applicants are unable to understand how preventing "gate oxide film of the initial input stage logic circuit from deterioration or breaking by reducing the value of the surge voltage Examiner's reasoning assertion" supports the assertion made by the Examiner that Matsuo suggests or teaches increasing the "gate capacitance". Applicants submit that Stein is directed at reducing output switching noise (1:6-9; and 2:1-3). Matsuo, on the other hand, is directed at preventing "a gate oxide film from deteriorating or breaking caused by plasma charged etching thereof..." (Abstract). Neither Stein, nor Matsuo, whether taken alone, or in combination, teach or suggest "the diodes contributing additional capacitance to the RC delay", as recited in part, in

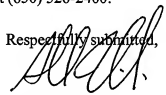
amended claim1. Therefore, contrary to the Examiner's assertion, no motivation exist to combine Stein with Matsuo.

Furthermore, combining Matsuo with Stein limits the maximum voltage that the transistor gates, as disclosed by Stein, can receive. This limit is defined by the reverse breakdown of the diodes of Matsuo. Accordingly, combining Matsuo with Stein, as best understood, limits the utility of Stein's transistor. Therefore, for this additional reason, the requisite motivation to combine Matsuo with Stein is not only lacking but also appears to teach away from Stein.

In view of the foregoing, Applicants believe all claims 1-3 and 5-6 now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 326-2400.

Respectfully submitted,



Ardeshir Tabibi
Reg. No. 48,750

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
AT:deh
60737238 v1